M.TECH PROGRAMME in
VLSI DESIGN
DEPARTMENT OF EIE

CENTURION UNIVERSITY OF TECHNOLOGY
MANAGEMENT, ODISHA
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<tr>
<th>Code</th>
<th>Subject</th>
<th>L-T-P</th>
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<tbody>
<tr>
<td>MTVD 1101</td>
<td>Analog VLSI Circuits</td>
<td>3-1-0</td>
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<td>MTVD 1201</td>
<td>VLSI Technology</td>
<td>3-1-0</td>
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<td>MTVD 1102</td>
<td>Semiconductor Device Modelling.</td>
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<td>MTVD 1202</td>
<td>CAD for VLSI.</td>
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<td>MTVD 1103</td>
<td>VLSI SYSTEM AND ARCHITECTURE</td>
<td>3-1-0</td>
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<td>MTVD 1203</td>
<td>Digital VLSI circuit.</td>
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<td>VDPE 1101</td>
<td>Elective---1 [ANY ONE]</td>
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<td>VDPE 1201</td>
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<td>VDPE 1103</td>
<td>VLSI Digital Signal Processing System</td>
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<td>2. HDL and High Level Synthesis.</td>
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<td>VDPE 1111</td>
<td>VLSI Testing</td>
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<td>3. VLSI and MEMS packaging.</td>
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<td>VDPE 1112</td>
<td>Elective---2 [ANY ONE]</td>
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<td>VDPE 1211</td>
<td>Elective --- 4 [ANY ONE]</td>
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<tr>
<td>VDPE 1113</td>
<td>1. RF and mixed Signal Integrated Circuits</td>
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<td>1. ASIC and SOC design</td>
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<td>VDPR 1107</td>
<td>Solid State circuit Lab</td>
<td>0-0-3</td>
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<td>VDPR 1207</td>
<td>2. Emerging Topic in IC design</td>
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<td>VDPT 1108</td>
<td>Seminar ( Pre-thesis work)-1</td>
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<td>VDPT 1208</td>
<td>3. Microsystems-Principle Design and Application</td>
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<td>VDCV 2101</td>
<td>Low Power VLSI Design</td>
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<td>VDPT 2201</td>
<td>Thesis / Project (Part-2)</td>
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<td>VDPE 2101</td>
<td>Elective --- 5 [ANY ONE]</td>
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<td>1. Introduction to Nano electronics.</td>
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<td>VDPT 2102</td>
<td>1. Statistical Signal Processing.</td>
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Semester credits 24

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Semester credits 20

Total cumulative Credits (4 semesters) 88
MTVD 1101 Analogue VLSI Circuit (3 – `1 – 0)

MODULE – I (11 hours)

Introduction:
The MOS Transistor, I-V Characteristics, Equivalent Circuits, Noise

Resistor, Capacitors and Switches:
Integrated Resistors, Integrated Capacitors, Analog Switches, Layout of Switches

Basic Building Blocks:
Inverter with Active Load, Cascode, Cascode with Cascode Load, Source Follower, Threshold Independent Level Shift, Improved Output Stages

MODULE – II (11 hours)

Current and Voltage Sources:
Current Mirrors, Current References, Voltage Biasing, Voltage References

CMOS Operational Amplifiers:
General Issues, Performance Characteristics, Basic Architecture, Two Stages Amplifier, Frequency Response and Compensation, Slew Rate

MODULE – III (12 hours)

Operational Amplifiers and OTAs
Design of Two Stage OTAs: Guidelines, Single Stage Schemes, Class AB Amplifiers, Fully Differential Op-Amps, Micro-Power OTAs, Noise Analysis, Layout

CMOS Comparators:
Performance Characteristics, General Design Issues, Offset Compensation, Latches

Textbooks:

Reference Books:

MTVD 1102 Semiconductor Device Modelling (3–1–0)

MODULE – I (13 hours)

Semiconductor Electronics Review:
Elements of Semiconductor Physics, Physical Operation of a PN Junction, MOS Junction, MS Junction

PN–Junction Diode and Schottky Diode:
DC Current-Voltage Characteristics, Static Model, Large-Signal Model, Small-Signal Model, Schottky Diode and its Implementation in SPICE2, Temperature and Area Effects on the Diode Model Parameters, SPICE3, HSPICE and PSPICE Models

Bipolar Junction Transistor (BJT):

MODULE – II (13 hours)

Junction Field-Effect Transistor (JFET):
Static Model, Large-Signal Model and its Implementation in SPICE2, Small-Signal Model and its Implementation in SPICE2, Temperature and Area Effects on the JFET Model Parameters, SPICE3, HSPICE and PSPICE Models

Metal-Oxide-Semiconductor Transistor (MOST):
Structure and Operating Regions of the MOST, LEVEL1 Static Model, LEVEL2 Static Model, LEVEL1 and LEVEL2 Large-Signal Model, LEVEL3 Static Model, LEVEL3 Large-Signal Model, The Effect of Series Resistances, Small-Signal Models, The Effect of Temperature, BSIM1, BSIM2, SPICE3, HSPICE and PSPICE Models

MODULE – III (14 hours)
BJT Parameter Measurements:
Input and Model Parameters, Parameter Measurements

MOST Parameter Measurements:
LEVEL1 Model Parameters, LEVEL2 Model (Long-Channel) Parameters, LEVEL2 Model (Short-Channel) Parameters, LEVEL3 Model Parameters, Measurements of Capacitance, BSIM Model Parameter Extraction

Noise and Distortions:
Noise, Distortion Metal-Semiconductor Field-Effect Transistor (MESFET), Ion-Sensitive Field-Effect Transistor (ISFET) and Semiconductor-Controlled Rectifier (Thyristor):
The MESFET, The ISFET, The Thyristor

Textbooks:

Recommended Reading:

MTVD 1103 VLSI SYSTEM AND ARCHITECTURE (3-1-0)

Module-1(14 lect)
Behavior and Architecture: Dedicated and Programmable VLSI architectures, Instruction sets and through enhancement techniques (Parallelism, pipelining, cache, etc.)
CISC Architecture Concepts: Typical CISC instruction set and its VLSI implementation, RTlevel optimization through hardware flow charting, Design of the execution unit, Design of the control part (micro programmed and hard wired), handling exceptions: Instruction boundary interrupts, immediate interrupts and traps.

Module-2(14 lect)
RISC Architecture concepts: Typical RISC instruction set and its VLSI implementation, Execution pipeline, Benefits and problems of pipelined execution, Hazards of various types of pipeline stalling, concepts of scheduling (Static and dynamic) and forwarding to reduce / minimize pipeline stalls Exceptions in pipelined processors
DSP architecture concepts: Typical DSP instruction set and its VLSI implementation

Module-3(14 lect)
Dedicated Hardware Architecture Concepts: Example and Case studies
Dedicated DSP architecture Concepts: Synthesis, Scheduling and Resource allocation, Conventional Residue number, distributed arithmetic architecture

Future Trends
Text Books:
VDPE1101  Digital Integrated Circuit Design (3 – 1 – 0)

MODULE – I (13 hours)
Introduction, Design Metrics and Manufacturing Process:

The Devices:

The CMOS Inverters and CMOS Logic Gates – the Static View:
Introduction to CMOS Inverter, The Static CMOS Inverter – An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter, Introduction to Static CMOS Design, Complementary CMOS, Ratioed Logic, Pass-Transistor Logic

CMOS Inverter – the Dynamic View:

MODULE – II (13 hours)
Dynamic CMOS Logic, Timing Metrics:
Dynamic CMOS Design, CMOS Logic Design Perspectives, Timing Metrics: Timing Metrics for Sequential Circuits, Classification of Memory Elements

Static and Dynamic Sequential Circuit Static Latches and Registers, Dynamic Latches and Registers, Alternative Register Styles: Pulse Registers and Sense-Amplifier Based Registers, Pipelining: An Approach to Optimize Sequential Circuits – Latch Vs Register-Based Pipelines and NORA-CMOS – A Logic Style for Pipelined Structures, Nonbistable Sequential Circuits

Coping with Interconnect:
Introduction, Capacitive Parasitics, Resistive Parasitics, Inductive Parasitics, Advanced Interconnect Techniques, Networks-on-a-Chip

Timing Issues in Digital Circuits:

MODULE – III (14 hours)
Designing Arithmetic Building Blocks:

Designing Memory and Array Structures:
Introduction, The Memory Core, Memory Peripheral Circuitry, Memory Reliability and Yield, Power Dissipation in Memories, Case Studies in Memory Design: The PLA, A 4-Mbit SRAM and A 1-Gbit NAND Flash memory, Perspective: Semiconductor Memory Trends and Evolution

Validation and Test of Manufactured Circuits:
Introduction, Test Procedure, Design for Testability, Test Pattern Generation

Textbooks:

Recommended Reading:
VDPE 1102 VLSI Digital Signal Processing Systems (3 – 1 – 0)

**MODULE – I (11 hours)**

**Introduction to DSP System:**
Typical DSP algorithms, DSP application demands and scaled CMOS technology, Representation of DSP algorithms.

**Iteration Bound:**
Data-flow graph representations, Loop bound and iteration bound, Algorithms for computing iteration bound, Iteration bound of multirate data-flow graphs.

**Pipelining and Parallel Processing:**
Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power.

**Retiming:**
Definitions and properties, Solving systems of inequal

**MODULE – II (11 hours)**

**Unfolding:**
An algorithm for unfolding, Properties of unfolding, Critical path, unfolding and retiming, Applications of unfolding.

**Folding:**
Folding transformation, Register minimization techniques, Register minimization in folding architectures, Folding of multirate systems.

**Systolic Architecture Design:**
Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-matrix multiplication and 2D systolic array design, Systolic design for space representations containing delays.

**MODULE – III (12 hours)**

**Bit-Level Arithmetic Architecture:**
Parallel multipliers, Interleaved floor-plan and bit-plane-based digital filters, Bit-serial multipliers, Bit-serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic.

**Programmable Digital Signal Processors:**
Evolution of programmable digital signal processors, Important features of DSP processors, DSP processors for mobile and wireless communications, Processors for multimedia signal processing.

**Textbooks:**

**Recommended Reading:**

VDPE 11034 VLSI Testing (3 – 1 – 0)

**Module I [13 hours ]**

Introduction, Test Process and ATE (2 classes), Test Economics (1 class), Yield Analysis and Product Quality (1 class), Fault Modeling (2 classes), Logic Simulation (1 class), Fault Simulation (1 class), Testability Measures (2 classes), Combinational ATPG (3 classes).

**Module II [13 hours ]**

Sequential ATPG (3 classes), Memory Test (4 classes), Analog Circuit Test (4 classes), Delay Test (2 classes)

**Module III [12 hours]**
IDDQ Testing (1 class), Design for Testability (3 classes), Built-In Self-Test (3 classes), Boundary Scan (2 classes), Analog Test Bus (1 class), System Test and Core Test (2 classes)

Textbook:


Reference Books:


VDPE 1111 RF and Mixed-Signal Integrated Circuits (3 – 1 – 0)

MODULE – I (13 hours)

Introduction: Overview of wireless principles, Characteristics of passive IC components – resistors, Capacitors, Inductors, Transformers, Interconnect at RF and high frequencies, Skin effect.

Bandwidth Estimation Techniques: Method of open-circuit time constants, Method of short-circuit time constants, Rise time, Delay and Bandwidth.

High-frequency Amplifier Design: Zeros as bandwidth enhancers, Shunt-series amplifier, Bandwidth enhancement with $f_T$ doublers, Tuned amplifiers, Neutralization and unilateralization, Cascaded amplifiers, AM-PM conversion.

MODULE – II (13 hours)

Voltage Reference: Review of diode behavior, Diodes and Bipolar Transistors in CMOS technology, Supply-independent bias circuits, Bandgap voltage reference, Constant-$g_m$ bias.


MODULE – III (14 hours)

Mixers: Mixer fundamentals, Non-linear systems as linear mixers, Multiplier-based mixers, Sub-sampling mixers, Diode-ring mixers.

RF Power Amplifiers: Classes of power amplifiers, RF power amplifier design example, Power amplifier characteristics and Design consideration.

Phase-Locked Loops (PLL): Introduction to PLL, Linearized PLL models, Some noise properties of PLLs, Phase detectors, Sequential phase detectors, Loop filters and charge pumps, PLL design examples.

Oscillators and Synthesizers: Problems with purely linear oscillators, Describing functions, Resonators, Tuned oscillators, Negative resistance oscillators, Frequency synthesis.

Textbooks:


Recommended Reading:

VDPE 1112   VLSI Physical Design   (3 – 1 – 0)

MODULE – I (11 hours)

VLSI Physical Design Automation:
VLSI Design Cycle, Physical Design Cycle, Design Styles, System Packaging Styles, Historical Perspectives, Existing Design Tools

Design and Fabrication of VLSI Devices:
Fabrication Materials, Transistor Fundamentals, Fabrication of VLSI Circuits, Design Rules, Layout of Basic Devices

Fabrication Process and its Impact on Physical Design:

MODULE – II (11 hours)

Data Structure and Basic Algorithms:
Basic Terminology, Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithm for Physical Design

Partitioning:
Problem Formulation, Classification of Partitioning Algorithms, Group Migration Algorithm, Simulated Annealing and Evolution, Other Partitioning Algorithms, Performance Driven Partitioning

Floor Planning and Pin assignment:
Floor Planning, Chip Planning, Pin Assignment, Integrated Approach

MODULE – III (12 hours)

Placement:
Problem Formulation, Classification of Placement Algorithms, Simulation Based Placement Algorithms, Partitioning Based Placement Algorithms, Other Placement Algorithms, Performance Driven Placement

Over-the-Cell Routing and Via Minimisation, Clock and Power Routing:
Over-the-Cell Routing, Via Minimisation, Clock Routing, Power and Ground Routing

Physical Design Automation of FPGAs:
FPGA Technologies, Physical Design Cycle for FPGAs, Partitioning, Routing

Physical Design Automation of MCMs:
MCM Technologies, MCM Physi

Text Books:


Reference Books:

MODULE – I (11 hours)
Basic Concepts, Quality and Reliability Assurance of Complex Equipments and Systems:
Introduction, Basic Concepts, Basic Tasks and Rules for Quality and Reliability Assurance of Complex Equipments and Systems

Probability Theory, Stochastic Process and Mathematical Statistics for Reliability Analysis:

Reliability Analysis During the Design and Development Phases:
Introduction, Predicted Reliability of Equipments and Systems with Simple Structure, Reliability of Systems with Complex Structure, Reliability Allocation, Mechanical Reliability, Drift Failure, Failure Mode Analyses, Reliability Aspects in Design Reviews

MODULE – II (11 hours)
Qualification Tests for Components and Assemblies:
Basic Selection Criteria for Electronic Components, Qualification Tests for Complex Electronic Components, Failure Modes, Failure Mechanisms, and Failure Analysis of Electronic Components, Qualification Tests for Electronic Assemblies

Maintainability Analysis:
Maintenance and Maintainability, Maintenance Concepts, Maintainability Aspects in Design reviews, Predicted Maintainability, Basic Models for Spare Part Provisioning, Cost Considerations

Design Guidelines for Reliability, Maintainability and Software Quality:
Design Guidelines for Reliability, Design Guidelines for Maintainability, Design Guidelines for Software Quality

MODULE – III (12 hours)
Reliability and Availability of Repairable Systems – II:

Statistical Quality Control and Reliability Tests:

Quality and Reliability Assurance During the Production Phase:
Basic Activities, Testing and Screening of Electronic Components, Test and Screening Strategies, Economic Aspects, Reliability Growth

Text Books:

Reference Books:
Course: M. Tech (VLSI Design) 1st semester

Solid state circuit Lab (0-0-3) 2 credit [0-0-3]

Solid State Lab

At least 8 experiments out of 10.

1. Program to compute Number of atoms/cm$^3$ in cubic crystals of silicon atom
2. Program to plot f(E) versus Energy for different temperatures
3. Compute & plot Vbi as a function of doping (NA or ND)
4. Program to generate an energy band diagram of a pn junction
5. Program to construct a plot of a square law relationship (IDsat/IDO versus VG/VP) of FET
7. Design of simple current mirror circuit.
8. Design of a simple ring oscillator.
9. Design of different common source amplifier circuits.
10. Design of different common drain amplifier circuits.

2nd semester

MTVD 1201 VLSI Technology (3 – 1 – 0)

MODULE – I (11 hours) Introduction:
Moore’s Law and material processing, Defects in crystals, Eutectic phase diagram, Solid solubility, Homogeneous nucleation, Heterogeneous Nucleation, Growth processes

Crystal Growth:
Necking and dislocation free CZ crystal growth, Segregation of impurities along length and diameter, Defects in CZ crystals, FZ Crystal growth

Epitaxy:
Vapour phase epitaxy, LPE, MBE, CVD deposition of Polysilicon, SILOX Process

Diffusion:
Constant & limited source diffusion, Concentration dependent diffusion, Field assisted diffusion, Junction depth, Open tube and closed tube diffusion, Diffusion sources.

MODULE – II (11 hours)

Ion Implantation:
Basic process, Ion Implantation Systems, Ion penetration and profile, Ion Implantation Damage, Annealing

Oxidation:
Purpose, Dry and wet oxidation, Deal-Grove model, Oxidation system, Properties of oxides – Masking and charges in oxides

Deposition Processes:
Fundamentals of vacuum systems, Vacuum evaporation of thin films, DC and RF Sputtering of thin films, Interconnects, Contacts and dielectrics in IC Fabrication, Deposition of Silicon Nitride, Silicides and insulating layers
Lithography:

MODULE – III (12 hours)

Etching:
Wet Etching, Isotropic and Anisotropic Etching, Plasma Etching, Reactive Ion Beam Etching.

IC Process Integration:
Bipolar Transistor Fabrication, Isolation techniques, P-MOS, N-MOS and C-MOS processes, IC Fabrication Process Integration, IC Process Yield and Reliability

MEMS Fabrication Processes:
Micro machining, Bulk Micro machining, Surface Micro machining, Deep RIE, Advanced Lithography, HEXIL & SCREAM Process, Polymer molding and LIGA Process

Text Books:

Reference Books:

MTVD 1202 CAD FOR VLSI CIRCUITS (3-1-0)

Module-1(15 lect)

VLSI DESIGN METHODOLOGIES

DESIGN RULES
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction

Module-2(12 lect)

DESIGN RULES – placement and partitioning - Circuit representation - Placement algorithms - partitioning

FLOOR PLANNING
Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

Module-3(16 lect)

SIMULATION
Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

MODELING AND SYNTHESIS

REFERENCES

MTVD 1203 Digital VLSI Circuit (3-1-0)

Module - I (15 hours)
Introduction, Historical perspective, VLSI Design methodologies, VLSI Design Flow, Design Hierarchy, Design Styles, CAD Technology. Fabrication of MOSFETS, Fabrication processes, NMOS Fabrication, CMOS n-well process, Layout Design rules, Stick Diagrams, Full Custom Mark Layout Design, MOS Transistor, Review of structure and operation of MOSFET (n-MOS enhancement type), CMOS, MOSFET v-I characteristics, MOSFET scaling and small geometry effects, MOSFET capacitances, Modeling of MOS Transistors - Basic concept the SPICE level-1 models, the level –2 and level –3 model equations.
MOS Inverters: Basic NMOS inverters, characteristics, inverters with resistive load and with n-type MOSFET load, CMOS inverter and characteristics.

Module - II (15 hours)
MOS inverters: Switching characteristics and interconnect effects: Delay time definitions and calculation, inverter design with delay constraints, estimation of parasitics switching power dissipation of CMOS inverters.
Combinational MOS logic circuits, CMOS logic circuits, state style, complex logic circuits, pass transistor logic, sequential logic circuit – introduction, SR latch, clocked latch & flip-flop circuits, CMOS D latch and edge triggered flip-flop.
Dynamics logic circuits: Dynamic logic, basic principles, high performance dynamics CMOS circuits, Dynamic Ram, SRAM, flash memory.

Module - III (12 hours)
Systems Design method, design strategies, concept of FPGA, standard cell based design, design capture tools, hardware definition languages such as VHDL and packages. Xilinx (introduction), introduction to IRSIM and GOSPL (open source packages), design verification and testing, simulation at various levels including timing verification, faults models. Design strategies for testing chip level and system level test techniques.

Text Books:
1. CMOS Digital integrated Circuits – Analysis & Design – Sung Mo-Kang & Yussuf Leblebici, TMH.
2. VHDL Programming by example – Perry TMH.

VDPE 1201 Analogue and Mixed-Signal Testing (3 – 1 – 0)

MODULE – I (11 hours)

MODULE – II (11 hours)
Sampling Theory – Analog measurements using DSP, Sampling and reconstruction, Repetitive sample sets, Synchronisation of sampling systems, DSP-Based Testing – Advantages of DSP-based testing, Digital signal processing, Discrete-time transforms, The inverse FFT, Analog Channel Testing – Overview, Gain and level tests, Phase tests, Distortion tests, Signal rejection tests, Noise tests, Simulation of analog channel tests, Sampled Channel Testing – Overview, Sampling considerations, Encoding and decoding, Sampled channel tests, Focused Calibrations – Overview, DC calibrations, AC amplitude calibrations, Other AC calibrations, Error cancellation techniques.

MODULE – III (12 hours)
DAC Testing – Basics of converter testing – intrinsic parameters versus transmission parameters, Comparison of DACs and ADCs, DAC failure mechanism, Basic DC tests, Transfer curve tests, Dynamic DAC tests, DAC architecture – Resistive divider DACs, Binary-weighted DACs, PWM DACs, Sigma-delta DACs, Compressed DACs, Hybrid DAC architecture, Tests for common DAC applications – DC references, Audio reconstruction, Data modulation, Video signal generators, ADC Testing – ADC testing versus DAC testing, ADC code edge measurements – Edge code testing versus center
code testing, Step search and binary search methods, Servo methods, Linear ramp histogram method, conversion from histograms to code edge transfer curves, Accuracy limitations of histogram testing, Rising ramps versus falling ramps, sinusoidal histogram method, DC tests and transfer curve tests, Dynamic ADC tests, ADC architecture – Successive approximation architecture, Integrating ADCs (Dual slope and single slope), Flash ADCs, Semiflash ADCs, PDM (sigma-delta) ADCs, Test for common ADC applications – DC measurements, Audio digitization, Data transmission, Video digitization, DIB Design – DIB basics, Printed circuit boards, DIB traces, shields and guards, Transmission lines, Grounding and power distribution, BIB components, Common DIB circuits, Common DIB mistakes, Design for Test (DfT) – Overview of DfT and BIST, Advantages of DfT, Digital scan, Digital BIST, Digital DfT for mixed-signal circuits, Mixed-signal boundary scan and BIST, Adhoc mixed-signal DfT, Subtle forms of analog DfT, IDDOQ testing.

Text Books:


Recommended Reading:


**VDPE 1202  HDL and High Level Synthesis  (3 – 1 – 0)**

**MODULE – I (13 hours)**

Structured Design Concepts:

Design Tools:
CAD Tool Taxonomy, Schematic Editors, Simulators, The Simulation System, Simulation Aids, Applications of Simulation, Synthesis Tools

Basic Features of VHDL:
Major Language Constructs, Lexical Description, VHDL Source File, Data Types, Data Objects, Language Statements, Advanced Features of VHDL, The Formal Nature of VHDL, VHDL 93

Basic VHDL Modeling Techniques:
Modeling Delay in VHDL, The VHDL Scheduling Algorithm, Modeling Combinational and Sequential Logic, Logic Primitives

**MODULE – II (13 hours)**

Algorithmic Level Design:
General Algorithmic Model Development in the Behavioral Domain, Representation of System Interconnections, Algorithmic Modeling of Systems

Register Level Design:
Transition from Algorithmic to Data Flow Descriptions, Timing Analysis, Control Unit Design, Ultimate RISC Machine

Gate Level; and ASIC Library Modeling:
Accurate Gate Level Modeling, Error Checking, Multivalued Logic for Gate Level Modeling, Configuration Declarations for Gate Level Models, Modeling Races and Hazards, Approaches to Delay Control

HDL-Based Design Techniques:
Design of Combinational Logic Circuits, Design of Sequential Logic Circuits

**MODULE – III (14 hours)**

ASICs and the ASIC Design Process:
What is an ASIC?, ASIC Circuit Technology, Types of ASICs, The ASIC Design Process, FPGA Synthesis

Modeling for Synthesis:
Behavioral Model Development, The Semantics of Simulation and Synthesis, Modeling Sequential Behavior, Modeling Combinational Circuits for Synthesis, Inferred Latches and Don’t Cares, Tristate
Circuits, Shared Resources, Flattening and Structuring, Effect of Modeling Style on Circuit Complexity

Integration of VHDL into a Top-Down Design Methodology:
Top-Down Design Methodology, Sobel Edge Detection Algorithm, System Requirements Level, System Definition Level, Architecture Design, Detailed Design at the RTL Level, Detailed Design at the Gate Level

Synthesis Algorithms for Design Automation:

Textbooks:

Recommended Reading:

VDPE 1203 VLSI and MEMS Packaging (3 – 1 – 0)

MODULE – I (11 hours)
Introduction: Basics of Electronic Packaging, Packaging Hierarchy in Electronic Systems, Functions of Packaging

Electric Considerations for Electronic Packaging: Electric Field Interference, Magnetic Field Interference, Noise performance due to passive components - Cabling, Shielding and Grounding/filtering/shielding/screening and surge protection/suppression, noise suppression


IC Packaging: Integrated Circuit Packages, Solder bumps, Direct Chip Attach, Multi-chip modules.

MODULE – II (11 hours)
IC Packaging (Continued): Microvia technology, LTCC


PCB Fabrication and Design: PCB technology trends, multi-layer boards, Design CAD tool for PCB design, artwork and layout, general rules, design rules for PCB’s for digital circuits, high frequency, analog and mixed signal circuits, power and microwave applications, Surface mount Technology

MODULE – III (12 hours)

Hybrid Electronic Packaging: Advantages of Hybrid packaging, Hybrid Fabrication Technology: Screen printing, conducting, resistive, dielectric and solder pastes, drying and firing, Hybrid assemblies

MEMS Packaging: MEMS Packaging Issues, Die Level Packaging, Wafer Level Packaging, Micro assembled caps, Sealing

Text Books:

Recommended Reading:
VDPE 1211  **ASIC and SoC Design (3 – 1 – 0)**

**MODULE – I (11 hours)**
- **Introduction:** Voice over IP SOC, Intellectual Property, SOC Design Challenges, Design Methodology.
- **Overview of ASICs:** Introduction, Methodology and Design Flow, FPGA to ASIC Conversion, Verification.

**MODULE – II (11 hours)**
- **SOC Design and Verification:** Introduction, Design for Integration, SOC Verification, Set-Top-Box SOC, Set-Top-Box SOC Example. Summary. References.

**MODULE – III (12 hours)**
- **Low-Power Design Tools:** PowerTheater, PowerTheater Analyst, PowerTheater Designer.
- **Open Core Protocol (OCP):** Highlights, Capabilities, Advantages, Key Features. Phase-Locked Loops (PLLs): PLL Basics, PLL Ideal Behavior, PLL Errors.

**Text Books:**

**Recommended Reading:**

VDPE 1212  **Emerging Topics in IC Design (3 – 1 – 0)**

**MODULE – I (11 hours)**
- **Review of MOS circuits:** MOS and CMOS static plots, switches, comparison between CMOS and BI-CMOS.
- **MESFETS:** MESFET and MODFET operations, quantitative description of MESFETS.
- **MIS structures and MOSFETS:** MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.
MODULE – II (11 hours)
Short channel effects and challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization
Beyond CMOS: Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic .Defect tolerant computing,
Super buffers, Bi-CMOS and Steering Logic: Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

MODULE – III (12 hours)
Special circuit layouts and technology mapping: Introduction, Talley circuits, NAND-NAND, NOR-NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out.
System design: CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Design of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

Text Books:

Recommended Reading:

VDPE 1213 Microsystems–Principles, Design and Application (3 – 1 – 0)

MODULE – I (11 hours)
Introduction: MEMS, MEMS Processing, Micromachining, Wafer Bonding, LIGA, MEMS Examples, Scaling Laws
MEMS Sensor: Resistive and Capacitive methods, Strain gauges, Piezoresistivity, MEMS Capacitive Sensors. MEMS Position sensor, MEMS Pressure sensor
MEMS Sensor (Continued): MEMS Accelerometer, MEMS Gyroscope, MEMS Gas Sensors, Cantilever Sensors
MEMS Actuator: Electrostatic MEMS actuators, Comb drives, MEMS RF resonator, Scratch drive, Inchworm motor, Piezoelectric MEMS actuators, Thermal MEMS actuators, Magnetic MEMS actuators

MODULE – III (12 hours)
Optical MEMS: MEMS Infrared sensor, Digital Mirror Displays, Grating Light Valve Displays, Micro-optical elements

Text Books:
Course: M. Tech (VLSI design) 2nd semester

VLSI CAD LAB 2 credit [0-0-3]

At least 4 from each group-A & B and one from group-C.

Group-A

1. Study of PMOS & NMOS Characteristics using SPICE
2. Layout of Basic circuit elements NMOS, PMOS using L-Edit
3. Layout & Circuit Simulation of CMOS Inverter
4. Study the static behaviour of CMOS inverter w.r.t. VDD and Temperature
5. Study the Dynamic behaviour of CMOS inverter w.r.t. VDD

Group-B

6. Design a full adder using
   a. Dataflow modelling.
   b. Structural modelling

7. Design a 4-bit adder cum sub tractor using:
   (a) 4:1 MUX using the following: (a)dataflow (b)using when else (c) structural
   modelling using 2:1 MUX (d) behavioural modelling using (i)case statement (ii)
   if else statement (e)mixed style of modelling(use structural, behavioural, dataflow)

8. Design a Decoders
   a. (3 : 8) and Encoder (Gray to Binary)
   b. Design a BCD to 7-Segment Decoder.

10. Design of Flip-Flops: (a)S-R Flip Flop (b)J-K Flip Flop (c) D Flip Flop (d) T Flip Flop
11. Design of up/down counters in synchronous and asynchronous mode.

Group-C

12. Design a 16 bit FSR (Feedback shift register).
13. Design a 16 bit ALU for 32 different logic and arithmetic operations.

3rd Semester

MTVD 2101  LOW POWER VLSI DESIGN (3-1-0)

Module-1(15)
DEVICE & TECHNOLOGY IMPACT ON LOW POWER
Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging
Low power approaches. Physics of power dissipation in CMOS devices. Dynamic dissipation in
CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device
innovation.

SIMULATION POWER ANALYSIS AND PROBABILISTIC POWER ANALYSIS SPICE circuit
simulators, gate level logic simulation, capacitive power estimation, static state power, gate level
capacitance estimation,

Module-2(15)
Architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation
- Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.
LOW POWER DESIGN
Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library
Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre computation logic
Module-3(15)
LOW POWER ARCHITECTURE & SYSTEMS, LOW POWER CLOCK DISTRIBUTION
Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design- Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip and package co-design of clock network
ALGORITHM AND ARCHITECTURAL LEVEL METHODOLOGIES
Introduction, design flow, algorithmic level analysis and optimization, Architectural level estimation and synthesis.
REFERENCES:

VDPE 2101 Introduction to Nanoelectronics (3 – 1 – 0)

MODULE – I (11 hours)
Introduction to Nanoelectronics: The “top-down” approach, The “bottom-up” approach, Nanoelectronics and nanotechnology potential.
Classical Particles, Classical Waves and Classical Quantum Particles: Comparison of classical and quantum systems, Origin of quantum mechanics, Light as a wave and light as a particle, Electrons as particles and electron as waves, Wavepackets and uncertainty.
Quantum Mechanics of Electrons: General postulates of quantum mechanics, Time-independent Schrodinger’s equation, Analogies between quantum mechanics and classical electromagnetics, Probabilistic current density, Multiple particle systems, Spin and angular momentum.

MODULE – II (11 hours)
Tunnel Junctions and Applications of Tunneling: Tunneling through a potential barrier, Potential energy profiles for material interfaces, Applications of tunneling – Field emission, Gate-oxide tunneling and hot electron effects in MOSFETs, Scanning tunneling microscope, Double barrier tunneling and the resonant tunneling diode.
Coulomb Blockade and the Single-Electron Transistor: Coulomb blockade – Coulomb blockade in a nanocapacitor, Tunnel junctions, Tunnel junction excited by a current source, Coulomb blockade in a quantum dot circuit, The single electron transistor, Other SET and FET structures – Carbon nanotube transistor, Semiconductor nanowire FETs and SETs, Molecular SETs and molecular electronics.

MODULE – III (12 hours)

Models of Semiconductor Quantum Wells, Quantum Wires and Quantum Dots: Semiconductor heterostructures and quantum wells, Quantum wires and nanowires, Quantum dots and nanoparticles, Fabrication techniques for nanostructures – Lithography, Nanoimprint lithography, Split-gate technology, Self-assembly.


Text Books:

Recommended Reading:

Statistical Signal Processing (3 – 1– 0)

Module – 1 (9 hrs)


Module – 2 (18 hrs)


Module – 3 (11 hrs)

Text Book

Reference Books
Adaptive Signal Processing (3 – 1 – 0)

MODULE – I (11 hours)
Winer Filter: Linear Optimum Filtering, Principle of Orthogonality, Minimum Mean Square Error, Winer-Hopf Equation, Error Performance Surface. [Read Haykin: Chapter 2.1-2.5]
Linear Prediction: Forward Linear Prediction, Backward Linear Prediction, Properties of Prediction Error Filters. [Read Haykin: Chapter 3.1, 3.2, 3.4]

MODULE – II (11 hours)
Method of Steepest Descent: Basic Idea of Steepest-Descent Algorithm, Steepest-Descent Algorithm Applied to Winer Filter, Stability of Steepest-Descent Algorithm, Limitations of Steepest-Descent Algorithm. [Read Haykin: Chapter 4.1 – 4.3, 4.6]
Least-Mean Square Adaptive Filter: Overview, LMS Adaptation Algorithm, Application, Comparison of LMS With Steepest-Descent Algorithm. [Read Haykin: Chapter 5.1 – 5.3, 5.5]
Normalized Least-Mean Square Adaptive Filter: Normalized LMS Filter as the Solution to Constrained Optimization Problem, Stability of the NLMS. [Read Haykin: Chapter 6.1, 6.2]

MODULE – III (11 hours)
Frequency-Domain and Subband Adaptive Filters: Block Adaptive Filters [Read Haykin: Chapter 7.1]
RLS Adaptive Filters: Statement of Linear Least-Square Estimation Problem, Matrix Inversion Lemma, The Exponentially Weighted RLS Algorithm. [Read Haykin: Chapter 8.1, 9.1 – 9.3]
Kalman Filter: Recursive Minimum Mean-Square Estimation For Scalar Random Variable, Kalman Filtering Problem, Initial Conditions, Summary of Kalman Filter. [Read Haykin: Chapter 10.1, 10.2, 10.6, 10.7]

Text Books
1. Bernard Widrow and Samuel D. Stearns, Adaptive Signal Processing, Pearson Education
2. Simon Haykin, Adaptive Filter Theory (Fourth Edition), Pearson Education