Post Graduate Diploma in VLSI Design

(One year programme)

Centre of Excellence for Electronic Design & Manufacturing

Centurion University of Technology & Management

2018

Post Graduate Diploma in VLSI Design

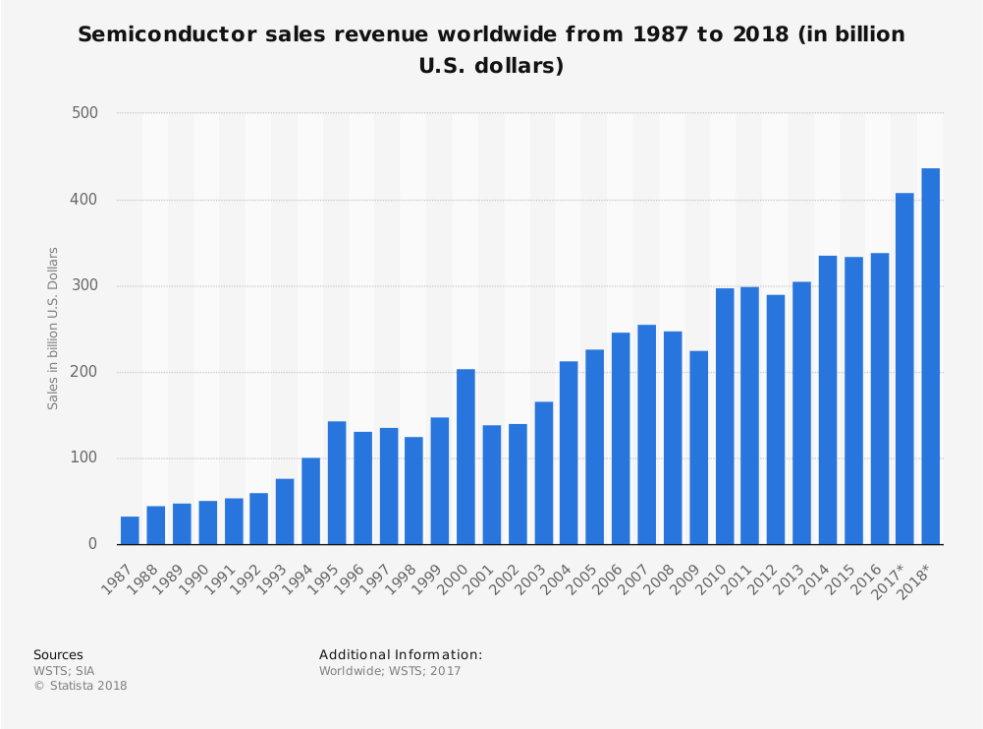
Mission:

- To strive to produce the highest quality engineers in the field VLSI Design and System Design – imbibed with a culture of innovation, and thus excel in the industry.
- To provide a unique balance between theory/practice and project-based training using industry's state-of-the-art EDA tools and the best practices.

The program is offered in collaboration with Tessolve Semiconductor India Pvt. Ltd, world's leading provider of end-to-end semiconductor, system and embedded solutions. For more details, visit www.tessolve.com.

Motivation: Significant Opportunities in Career growth in VLSI/Semiconductor Industry

The world around us is electronics and semiconductors. The gadgets that we use every day come to life due to electronics and semiconductor. Here is the growth of semiconductor sales worldwide since 1987. With the advent of big data, self-driving cars, robots, IoT, blockchain, bitcoins, the industry is now rediscovering itself, reinventing itself.



The career growth plan is multifold –

1. Work in one or more of the following areas:
    a. Architecture, Design, Verification, Emulation, Design-for-test, Physical Design, Post-silicon bring-up
    b. Work at Logic Level as a digital engineer or transistor level as an analog engineer
    c. Work as a semiconductor process engineer
2. On a long-term career growth, be in engineering, engineering management, research for future innovation, or sales and business development.

Program:

- PG Diploma in VLSI Design, Duration 1 year.
    1. With emphasis on Design
    2. With emphasis on Verification

Program Objective:

To make young engineering and science graduates ready for VLSI industry.

Program Overview:

The course is structured based on the need of today's demanding VLSI industry. The coursework covers the basic skills in Linux, scripting, programming and project management that is required to effectively perform the VLSI tasks. The students are expected to put in extra time to hone their skills on the basics. The second phase in the coursework covers logic design, SoC flow, Verilog HDL. Beyond these two steps, the students can branch into **either design or verification** based on their passion. Once the students cover their respective curriculum in either design or verification, students are then introduced industry standard high-speed protocols as a part of their project internship.

A- Phase 1: Basic skills in Linux, Scripting, Programming and Project management
B- Phase 2: Logic design, SoC flow, Verilog HDL
C- Phase 3: Choice of either Design or Verification
D- Phase 4: Industry Internship – Learn industry protocols and do one or more projects

Expectation from Students:

The fact that you are committing to the rigors of the VLSI curriculum, you are required to put in all-out effort to learn in this course. You will need to consider this course as a giant guide to enter the industry. You will need to put in lot of hours of self-study outside of the classroom, come up with the list of questions, and meet the faculty engineers during office hours to go over them.

Program Duration:

1-year

Credit: 48

Admission

- All interested students will go through a written test to gauge the knowledge base where they are in, and accordingly the program will recommend the effort that the students.
- Due to limited seating, only the top 20 students will be into the program.

Eligibility

- Bachelor's degree in Engineering / Technology or equivalent degree (e.g. AMIE etc.) in Electronics/Electrical and Electronics/Electronics and Instrumentation/Electronics and Communication/Electronics and Telecommunication/Electronics and Computer/ Instrumentation/Information Technology/Computer and Communication/Computer Science/Computer Engineering or related areas with minimum CGPA of 6 or 60% of marks or First Class in qualifying examination.
- ME/MTech/MS in any ECE/CSE/EEE/IT specialization
- MSc in Engineering Science/Electronics/Electronics and Communication/Computer Science/IT/Physics with specialization in Electronics/Information Technology with minimum CGPA of 6 or 60% of marks or First Class in qualifying examination.

Who Will Teach the Course?

The experienced engineers from Tessolve Semiconductor and the highly qualified faculties of Centurion University of Technology and Management will jointly deliver the course.

Award of degree

After successful completion of course, candidates will be awarded with "Post Graduate Diploma in VLSI Design" by Tessolve Semiconductor and Centurion University of Technology and Management.

Attendance:

100% attendance in each subject is mandatory.

Evaluation and Assessment

Assessment and evaluation will be carried out as per the university examination rules and regulation. Course evaluation will be done in two parts

1. Continuous Assessment – 60 Marks
2. Course End Examination – 40 Marks

Continuous Assessment: This evaluation process is to be done by the respective subject faculty at regular intervals during the progression of subject. The 60 marks is further divided in two parts:

1. Lab Test – 40 Marks
    a. 5 lab test of 8 Marks each
2. Internal Test – 20 Marks
    a. Class Test – 10 Marks (mandatory 3 class tests at regular interval and average of three will be taken)
    b. Surprise Test/ Quizzes – 5 Marks
    c. Assignment/Viva/Seminar – 5 Marks

Weightage for each component is as follows:

1. Lab Examination: 40%
2. Internal Examination: 20%
3. Course End Theory Examination: 40%

Examination may be conducted for higher number of marks but the marks obtained by the student will be scaled down. Internal test will be done by the respective subject faculty and Lab test will be done by the subject faculty with the help of programme coordinator.

Course End Examination: This may be written theory examination to be conducted under the supervision of programme coordinator at the completion of each subject.

Evaluation of Industry Internship Project

I. Weekly report on internship project: 20% (to be examined by the supervisor)
II. Supervisor: 30%

III. Final report: 30% (to be examined by expert committee)
IV. Project Presentation and Viva: 20% (to be examined by expert committee)

At the end of course, evaluated marks of all subjects is to be submitted to QA Cell of CUTM for the publication of results and award of degree certificate.

Passing Criteria: Pass marks for theory, practice or lab and project will be as follows:

Theory	**Practice/Lab**	**Project**
40%	50%	50%
Candidate has to get pass percentage in individual components		

Minimum pass marks to be scored in each component to pass any subject:

- For 40 marks theory examination: 16
- For 40 marks lab test: 20
- For 20 marks internal test: 10

Course Structure

Semester-I

Course Code	Course Title	Course Type	Credits
PGVL0401	Linux Shell Scripting, Perl, Python	Theory + Practice	2
PGVL0402	Programming Fundamentals	Theory + Practice	3
PGVL0403	Advanced Digital Design	Theory + Practice	3
PGVL0404	System Architectures	Theory + Practice	4
PGVL0405	Verilog HDL	Theory + Practice	4
PGVL0406	CMOS VLSI and ASIC Design	Theory + Practice	3
PGVL0201	Soft Skills	Practice	2
	Elective 1		4
	Elective 2		2
Semester - II			
PGVL0801	Industry Internship Project	Project	20

Elective

Course Code	Course Title	Course Type	Credits
PGDE0401	Chip Design Concepts	Theory + Practice	4
PGDE0402	System Verilog	Theory + Practice	4
PGDE0403	HDL Simulation and Synthesis	Theory + Practice	3
PGDE0404	Verification using UVM	Theory + Practice	3

Syllabus

Linux Shell Scripting, Perl and Python

Subject Name	Code	Type of course	Credit	Hours
Linux Shell Scripting, Perl and Python	PGVL0401	Theory + Practice	2	40

- Vi Editor, Linux commands, File handling utilities, Security by file permissions, Process utilities, Disk utilities, Filters, Text processing utilities and Backup utilities, Linux scripting language, sed – scripts, operation, addresses, commands, applications, awk – execution, fields and records, scripts, operation, patterns, actions, functions, using system commands in awk.
- The Shell, shell responsibilities, pipes and input Redirection, output redirection, here documents, running a shell script, shell programming, shell meta characters, file name substitution, shell variables, command substitution, shell commands, the environment, quoting, test command, control structures, shell scripting, interrupt processing, functions, debugging shell scripts.
- File Concept, File System Structure, File Attributes, File types, Library functions, the standard I/O and formatted I/O in C, stream errors, kernel support for files, System calls, file descriptors, low level file access – File structure related system calls (File APIs), file and record locking.
- Perl
- Python
- Lab Practice

Books:

1. Beginning Linux Programming, 4th Edition, N.Matthew, R.Stones,Wrox, Wiley India Edition.
2. Linux System Programming, Robert Love, O'Reilly, SPD.

Programming Fundamentals

Subject Name	Code	Type of course	T-P-P	Hours
Programming Fundamentals	PGVL0402	Theory + Practice	1-2-0	80

C Primer

- Data types, operators, control statements, loops
- Arrays, array of pointers, passing array of pointers to functions, memory allocation, Conditional compilation and recursion, calling same function, Functions, strings,
- Structures & unions,
- File handling.

Programming in C++

- OOPs concept, C++ characteristics, data types. Functions and variables, dynamic creation and derived data, arrays and strings in C++, qualifiers.
- Classes & Objects, classes and encapsulations, member functions, instantiation using classes and constructors, destructor.
- Operator overloading, initialization, assignments. Polymorphism, Inheritance, base and derived classes, constructor and destructor calls.
- Lab Practice

Books:

1. E. Balaguruswamy “Programming in C”, Tata McGraw Hill3rdedition
2. Y. Kanetkar, “Let us C”, BPB Publications-9th edition.
3. H. Scheldt, “C - The Complete Reference”, Tata McGraw Hill
4. B.W. Kernighan & D.M. Ritchie, "C Programming Language", PHI.
5. Schaum Series-“C Programming”-Gotterfried
6. Object Oriented Programming with C++, E. Balagurusamy
7. Object-oriented programming in Microsoft C++, Robert Lafore

Advanced Digital Design

Subject Name	Code	Type of course	T-P-P	Hours
Advanced Digital Design	PGVL0403	Theory + Practice	2-1-0	80

- Number system, different coding style, Boolean algebra, K-map
- Combinatorial Logic Design
  - Combinational circuit design procedure. Circuit design from word description.
  - Full adder, 4-bit binary adder.
  - Multiplexer, multiplexer tree, logic function implementation using multiplexer
  - DE multiplexer
  - Decoder, decoder tree, logic function using decoder
  - Encoder, priority encoder
  - Multiplier
- Review of Sequential circuits: latches, flip-flops, latch using multiplexer, ripple counter, sequential counter, register.
- Sequential Logic Design: Finite State machines, Mealy and Moore type, FSM design of sequence detector, Counter, traffic light signal, vending machines and other real-world application.
- Design Issues:
  - Noise margins, power, fan-out
  - Design rules, metastability,
  - Skew, jitter, timing considerations,
  - Frequency divide,
  - Logic Hazards and glitches- static and dynamic hazard, hazard in combination circuit, fixing of static hazard, hazard in multi-level circuit, hazard in asynchronous sequential circuits.
- Asynchronous State Machine- cycle stealing using latch in synchronous circuits, Interfacing Asynchronous data flow
- Asynchronous FIFO design
- Case study of digital design circuits

Books:

1. Advanced Chip Design: Practical Examples in Verilog, Kishore Kumar Mishra, Create Space Independent Publishing Platform, (2013).
2. Advanced Digital Design with the Verilog HDL; Michael D. Ciletti; 2009,1st edition, PHI,2010.

3. Digital Design, by M. Morris Mano and Michael D. Ciletti, Pearson Edu. India
4. Digital Systems- Principles and Applications, R. J. Tocci, N S. Widmer and G. L. Moss, 12th Edition, Pearson Education.
5. Digital Design – Principle & Practice, 3rd Edition by John F. Wakerly, Pub. Pearson Education.
6. Digital Principles and Applications, 6th Edition, Donald P. Leach, Albert Paul Malvino and Goutam Saha, Tata McGraw Hill Publishing Company Ltd., New Delhi.

System Architectures

Subject Name	Code	Type of course	T-P-P	Hours
System Architectures	PGVL0404	Theory + Practice	2-2-0	120

- Computer architecture
- Architecting for area, speed and power
- Introducing Interface bus protocols
  - High speed protocols includes DDR, and PCI Express
  - Low speed protocols include I2C, SDI, UART, SPI
- Introducing Internal bus protocols
  - AMBA AXI
  - AMBA CHI

Books:

1. Advanced Chip Design: Practical Examples in Verilog, Kishore Kumar Mishra, Create Space Independent Publishing Platform, (2013).
2. VLSI and Computer Architecture by Ravi Sankar and Eduardo B. Fernandez.
3. D A Patterson and I L Hennessy, "Computer Architecture: A Quantitative approach", Second edition, Margon Kaufmann, 1996

Verilog HDL

Subject Name	Code	Type of course	T-P-P	Hours
Verilog HDL	PGVL0405	Theory + Practice	1-2-0	80

- Introduction, level of abstraction, Verilog primitives, keywords, data types, nets and registers, arrays, Verilog Modules, ports types and declaration,
- Verilog Operators: Logical operators, Bitwise and reduction operators, Concatenation and conditional operators, Relational and arithmetic, Shift and equality operators, Operator execution order.
- Gate type, design hierarchy, gate delay, propagation delay, logic simulation, user defined primitive. Structural modelling and module instantiation.
- Assignments: Types of assignments, Continuous assignment, Procedural assignments: Blocking and non-blocking statements, begin-end, fork-join, Dataflow-level modelling: assignments.
- Behavioural modelling: Always, initial blocks, Flow Control, If-else, case, casex. Loops: while, for, repeat. Compiler directives, ifdef,
- Task and Functions
- Verilog system tasks and functions, writing tasks and functions.
- Combinational and sequential circuit design
- Logic synthesis, RTL synthesis, high-level synthesis, synthesis design flow.
- FSM design, memory modelling
- Specify block and Timing checks
- Verilog for Verification and Writing test benches, design verification and testing.
- RTL coding styles, unwanted latches, writing reusable codes.
- LAB Practice

Books:

1. Verilog HDL: A Guide to Digital Design and Synthesis; Samir Palnitkar; 2nd edition, Pearson Education, 2011
2. Advanced Chip Design: Practical Examples in Verilog, Kishore Kumar Mishra, Create Space Independent Publishing Platform, (2013).
3. Advanced Digital Design with the Verilog HDL; Michael D. Ciletti; 2009,1st edition, PHI,2010
4. Verilog HDL Synthesis: A Practical Primer; J. Bhasker; BSP Publishers, 2008.

CMOS VLSI and ASIC Design

Subject Name	Code	Type of course	T-P-P	Hours
CMOS VLSI and ASIC Design	PGVL0406	Theory + Practice	**2-1-0**	**80**

- MOS device: N-type and P-type MOS transistor. MOS structure, MOS operation, Threshold Voltage, drain current characteristics, transfer characteristics.
- Body bias effect, Channel length modulation, Latch-up effect, prevention of latch-up.
- Technology scaling and its effect on MOS device parameters and performances. Small geometry effect. Resistance and capacitance estimation of MOS device.
- CMOS Inverter, Voltage Transfer Characteristics (VTC), critical voltages, Noise margin. Ratioed and non-ratioed logic, saturated load logic, pseudo NMOS logic.
- CMOS inverter switching characteristics, rise, fall and propagation delay time. Estimation of interconnect parasitic, estimation of interconnect delay, Elmore delay model, insertion of buffer in long interconnect to reduce delay, crosstalk.
- Power dissipation in CMOS circuit, static and dynamic power, leakage currents and leakage power, minimization of leakage and dynamic power.
- CMOS combinational logic design, Design of Basic gates and Design of complex logic circuit, Device sizing of CMOS circuit.
- Spice Simulation: AC, AC and Transient analysis of CMOS circuits. Noise analysis of current and voltage.
- Layout design rule, Micron and Lambda based design rule, design rule check. Layout design of different library cell like NOT, NAND, NOR, Ex-OR etc. Fabrication process of NMOS, PMOS and CMOS. N-well CMOS fabrication process.
- Pass transistor, transmission gates, logic circuits using pass transistor and transmission gates.
- Issues of dynamic logic-charge sharing, charge leakage. CMOS circuit using dynamic logic, cascading of dynamic logic circuits, domino logic.
- Full custom IC design flow. Schematic, circuit simulation, layout design, DRC, electrical rule check, Layout Vs. Schematic(LVS), parasitic extraction, post-layout simulation and mask design.
- Design Issues: Antenna effect, Electro migration effect, Body effect, Inductive and capacitive cross talk and Drain punch through, etc.
- PLA and Memory

Books:

1. Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design,Tata McGraw-Hill Publishing Company Limited, 3rdEdition/4th Edition
2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits – A Design Perspective, PHI, 2nd Edition.
3. Wayne Wolf, Modern VLSI Design System – on – Chip Design, PHI, 4th Edition.
4. John P,Uyemura, CMOS Logic Circuit Design, Springer (Kluwer Academic Publishers),
5. Ken Martin, Digital Integrated Circuit Design, Oxford University Press,
6. K,Eshraghian and N,H,E,Weste, Principles of CMOS VLSI Design – a Systems Perspective, 2nd Edition, Addison Wesley, 1993
7. N. Weste, D. Harris and A. Chatterjee, CMOS VLSI Design: A Circuits and Systems Perspective, Pearson Education.

Soft Skill

Subject Name	Code	Type of course	T-P-P	Hours
Soft Skill	PGVL0201	Practice	**0-2-0**	**40**

Course outline

- Effective Speaking Skills
- Effective English writing skills,
- Interview skills,
- Resume writing skills,
- Do's and Don'ts during interview
- Project Management Skills
- Manners and Etiquette

Chip Design Concepts

Subject Name	Code	Type of course	T-P-P	Hours
Chip Design Concepts	PGDE0401	Theory + Practice	2-2-0	120

- Introduction to System on Chip (SOC), ASIC Design Flow.
- Anatomy of a SOC in terms of datapath- control paths, analog and digital blocks, I/O ring
- Design for testability (DFT):
  - Introducing the concepts: Internal Scan, Automatic Test Patter Generation and Simulation, Built-in-self-test (BIST), Boundary Scan, Tap Controller
  - Introducing the standards: IEEE 1149.1, IEEE 1149.6, IEEE 1500.
- FPGA Architecture: Programmable Logic Devices (PLDs), General structure and classification: SPLD, CPLD, PAL, PLA, FPGA etc. Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Applications of FPGAs. Xilinx FPGA Architecture: Features and architectures, Configurable Logic Blocks (CLBs), Input Output Blocks (I/OB), Block RAM, Programming interconnects, Digital Clock Manager (DCM), Power Distribution and configuration.
- Low power design techniques. Why low power? Sources of power dissipation, high performance design concepts. Low power design: circuit level and logic level. Low power architecture and low power clock distribution. Low leakage design techniques.
  - Unified Power Format (UPF) for low power design, IEEE1801 – introduction and overview, components of UPF, IP design using UPF, system design using UPF.

Books:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits – A Design Perspective, PHI, 2nd Edition.
2. N. Weste, D. Harris and A. Chatterjee, CMOS VLSI Design: A Circuits and Systems Perspective, Pearson Education.
3. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing, Kluwer Academic Publishers.
4. M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, Wiley-IEEE Press.
5. VLSI Test Principles and Architectures; Wang, Wu and Wen; Elsevier.

System Verilog

Subject Name	Code	Type of course	T-P-P	Hours
System Verilog	PGDE0402	Theory + Practice	2-2-0	120

- Introduction to verification, types of verification, anatomy of test bench. System Verilog for verification.:
- Different Data types, User-Defined and Enumerated Types: string data types, event data types, User-defined types, Enumerated types, Nets, reg, logic, Type casting, Constants, attributes, operators and expressions,
- Procedural statements and control flow, processes.
- Tasks, functions, Enhancements to tasks and functions, Task and function argument passing, Import and export functions, System Tasks and System Functions,
- Interface concepts, Interface declarations, using interfaces as MODULE ports, Instantiating and connecting interfaces, referencing signals within an interface, Interface modports, Using tasks and functions in interfaces, parameterized interfaces, virtual interfaces, Using procedural blocks in interfaces, Reconfigurable interfaces, Verification with interfaces
- OOPs Terminology, Implementation of OOPs Concepts in SV,
- Randomization and constraints: randomization in System Verilog, constraint details, controlling multiple constraints, common randomization problems, iterative and array constraints, random controls, random generators, random device configuration Fork Join (Join, Join_any, Join_none),
- Event controls, semaphores, Mailboxes, virtual interfaces, transactors,
- System Verilog for verification: Building verification environment, Testcases
- Code coverage and Functional Coverage: Coverage models, cover points and bins, cross coverage, Assertion,
- IPC.
- Lab Practice

Books:

1. SystemVerilog for Design, S. Sutherland, S. Davidmann and Peter Flake
2. SystemVerilog for Verification, CHoursis Spears, Synopsis Inc.
3. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features by Chris Spear & Greg Tumbush (3rd Edition)
4. System Verilog, 3.1a, Language reference manual.

HDL Simulation and Synthesis

Subject Name	Code	Type of course	T-P-P	Hours
HDL Simulation and Synthesis	PGDE0403	Theory + Practice	1-2-0	80

- The concept of Simulation, Types of simulation
- HDL Simulation and Modelling
- The Synthesis Concept, Synthesis of high level constructs
- Static Timing Analysis of Logic circuits
- Combinatorial Logic Synthesis
- State machine synthesis
- Hierarchical and flat designs, Constraining designs
- Pipelining, Resource sharing, Optimizing arithmetic expressions
- Advanced simulations
- Efficient coding styles, Coding for synthesis, Synthesis optimization
- Partitioning for synthesis, Floor planning & place and route optimization
- Design reuse, The Simulation and Synthesis Tools, FPGA synthesis and implementation
- Clock domains, Reset circuits

Books:

1. Verilog HDL Synthesis: A Practical Primer, J Bhaskar
2. High Level VLSI Synthesis, Raul Camposano, and Wayne Wolf, Springer
3. High-level Synthesis: Introduction to Chip and System Design, Daniel D. Gajaski, Nikhil D. Dutt, Allen C. –H. Wu and Steve Y. –L. Lin

Verification using UVM

Subject Name	Code	Type of course	T-P-P	Hours
Verification using UVM	PGDE0404	Theory + Practice	1-2-0	80

- UVM Basics: UVM TB Architecture, Creating UVCs and Environment, UVM simulation phases, Test Flow, transaction, Test bench and its component.
- Configuring UVM environment: Configuration, UVM Sequences, UVM sequencers, Connecting Device Under Test (DUT) -Virtual Interfaces, Virtual sequences and sequencers, predictor, monitor.
- Creating UVM environment: Building a Scoreboard, Building reusable environments, multiple sequences configuration.
- Hierarchy in UVM, UVM class factory overview, factory overrides, UVM reporting, UVM register model, Transaction Level Modelling (TLM).
- Creating test plan from specification, Coverage: Code coverage and Functional Coverage
- Assertion Based Methodology: Immediate assertion, simple assertions, sequences, sequence composition, assertion coverage
- Lab Practice

Books:

1. UVM 1.2 user's Guide
2. UVM 1.2 class reference
3. The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology, Ray Salemi
4. Getting Started with UVM: A Beginner's Guide by Vanessa R. Copper
5. A Practical Guide to Adopting Universal Verification Methodology (UVM) by Sharon Rosenberg & Kathleen A Meade (2nd Edition
6. System Verilog for Verification: A Guide to Learning the Test bench Language Features by Chris Spear & Greg Tumbush (3rd Edition)

SEMESTER -II

Subject Name	Code	Type of course	T-P-P
Industry Internship Project	PGVL0801	**Project**	**0-0-20**

The student will work on a state-of-the-art design and verification project in house at Tessolve Semiconductor or in any chip verification industry. At the end of internship programme the student has to submit internship and project report for evaluation.